Very Low-Loss Distributed X-Band and Ka-Band MEMS Phase Shifters Using Metal–Air–Metal Capacitors

Joseph S. Hayden, *Member, IEEE,* and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—2-bit wide-band distributed coplanar-waveguide phase shifters have been developed on a 500-μm quartz substrate for X- and Ka-band operation. The designs utilize microelectromechanical system (MEMS) switches in a distributed MEMS transmission line) periodically loaded by MEMS switches and high Q ($\geq$250 at 30 GHz) metal–air–metal capacitors. The MEMS switches are actuated by a $\pm$20-V voltage waveform using a high-resistance bias line. Estimated spring constant and switching time is 30 N/m and 9 μs, respectively. The Ka-band 2-bit design results in a reflection coefficient better than $-$11.5 dB, an average insertion loss of $-$1.5 dB and phase shifts of 0°, 89°, 180°, and 270° at 37.7 GHz. The X-band 2-bit design results in a reflection coefficient better than $-$12.5 dB, an average insertion loss of $-$1.2 dB and phase shifts of 0°, 94°, 176°, and 270° at 13.6 GHz. These results are very competitive with switched transmission-line and reflection-based phase shifters. The distributed design can be easily scaled to V- and W-band frequencies for wide-band low-loss performance.**

***Index Terms*—Microelectromechanical system (MEMS), microwave, phase shifter, switches, true-time delay.**

I. Introduction

DISTRIBUTED phase shifters operate on a principle of dispersion. By increasing the distributed capacitance on a transmission line (t-line), the phase velocity decreases, thus providing a differential phase shift. There have been many recent demonstrations of distributed microelectromechanical-system transmission line (DMTL) phase shifters using coplanar waveguide (CPW) and microstrip lines [1]–[8]. In the DMTL design, microelectromechanical system (MEMS) switches are used to change loading capacitance on a high-impedance t-line ($>$50 Ω) such that the return loss is within an acceptable range for the two phase states (with the MEMS switches in the up- and down-state positions). Generally, the loaded impedances are chosen to be 60 Ω (up-state position) and 41.7 Ω (down-state position) for a $-$15 dB of return loss per bit. The goal of the design is to provide the maximum amount of phase shift with the minimum amount of insertion loss and with a return loss of less than $-$10 dB over all possible phase states.

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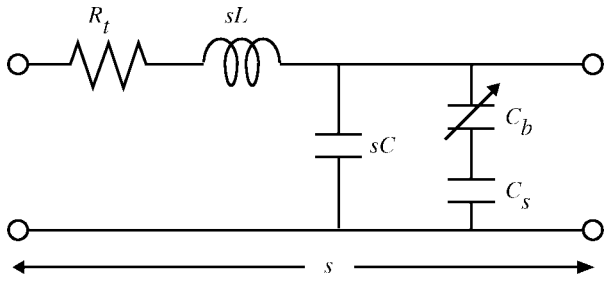


Fig. 1. Lumped model for one section of a DMTL phase shifter.

The Ka-band design described in this paper is the first demonstration of a DMTL phase shifter at 30–40 GHz and the first demonstration utilizing high-Q metal–air–metal (MAM) capacitors instead of the standard metal–insulator–metal (MIM) capacitors. The high-Q MAM capacitors are responsible for a drastic improvement in the performance of the DMTL phase shifter. Also, high-resistivity bias lines have been introduced for lower voltage actuation of the MEMS switches. The effect of the bias lines is discussed in Section V.

II. Closed-Form Design Equations

A short section (length $= s$) of a t-line in a DMTL phase shifter can be approximated as a lumped circuit consisting of an inductance sL (inductance of the t-line) in shunt with: 1) t-line capacitance sC and 2) MEMS switch capacitance C_b in series with a fixed capacitance C_s (Fig. 1). The loaded t-line impedances Z_u (up-state position) and Z_d (down-state position) and propagation velocity are given by

$$Z_{u,d} = \sqrt{\frac{sL}{sC + \dfrac{C_s C_b}{(C_s + C_b)}}} \tag{1}$$

$$v = \frac{1}{\sqrt{sL\left(sC + \dfrac{C_s C_b}{(C_s + C_b)}\right)}} \tag{2}$$

where C_b is around 20–50 fF in the up-state position and 1–3 pF in the down-state position for a Ka-band design. The following expressions, combined with the Bragg frequency f_B (see [6])

are solved to develop closed-form design equations for a DMTL phase shifter:

$$s = \frac{Z_d c}{\pi f_B Z_o \sqrt{\epsilon_{r,\text{eff}}}} \text{ meters} \tag{3}$$

$$C_{bu} = \frac{\left(Z_o^2 - Z_u^2\right) Z_d}{Z_o^2 Z_u^2 \pi f_B} \text{ farads} \tag{4}$$

$$C_r = \frac{Z_u^2}{Z_d^2} \frac{\left(Z_o^2 - Z_d^2\right)}{\left(Z_o^2 - Z_u^2\right)} \tag{5}$$

$$\Delta\phi = \frac{s\omega Z_o \sqrt{\epsilon_{r,\text{eff}}}}{c} \left(\frac{1}{Z_u} - \frac{1}{Z_d}\right) \text{ rad/section} \tag{6}$$

where Z_o and $c/\sqrt{\epsilon_{r,\text{eff}}}$ are the characteristic impedance and guided velocity of the high-impedance CPW line without any loading. C_{bu} is the capacitance of the MEMS switch in the up-state position, and C_r is the capacitance ratio of the MEMS switch ($C_r = C_{bd}/C_{bu}$). In this study, the Bragg frequencies are selected to be approximately 2.5 times the design frequencies at 10 and 30 GHz [3].

The design starts with the closed-form expressions for phase shift, MEMS separation, and loading capacitors, but true modeling is best achieved by the software package Sonnet,[1] a method-of-moments simulator that is found to produce accurate simulations of these distributed circuits. Typically, the Sonnet simulation is performed on only one unit cell and a multiple cell simulation is obtained by cascading the unit-cell S-parameters in a circuit simulator such as Agilent-ADS.[2]

The loss of the loading capacitor is modeled as a resistance R_p in parallel with C_s (or a resistance R_s in series with C_s). The corresponding t-line loss α has been calculated by several authors [3], [9], [10] and is

$$\alpha \cong \frac{R_t}{2Z_d} + \frac{R_s Z_d \omega^2 C_s^2}{2} \text{ Np/section} \tag{7}$$

or

$$\alpha \cong \frac{R_t}{2Z_d} + \frac{Z_d}{2R_p} \text{ Np/section} \tag{8}$$

where R_t is the unloaded t-line series resistance. The impedance Z_d is taken as the down-state loaded impedance when the static capacitor is connected to the t-line.

Consider for example X-band ($f_o = 10$ GHz, $f_B = 23$ GHz) and Ka-band ($f_o = 30$ GHz, $f_B = 67$ GHz) designs with loaded impedances of $Z_u = 60\ \Omega$ and $Z_d = 42\ \Omega$. The CPW line dimensions are 300/300/300 μm and 150/150/150 μm ($Z_o = 98\ \Omega, \epsilon_{r,\text{eff}} = 2.36$) with a measured unloaded line loss of 11.2 and 38.9 dB/m at 10 and 30 GHz, respectively. This results in $R_t = 250$ and $R_t = 860\ \Omega$/m, respectively. The corresponding spacing and loading capacitances are $s = 1{,}150\ \mu$m, $C_s = 267$ fF, and $s = 400\ \mu$m, $C_s = 93$ fF, respectively.

Table I shows the effect of the capacitor Q loss in relation to the other major contributor of DMTL loss, the loaded-line loss. It is clear that one needs $Q \geq 150$ for low-loss performance. For this reason, MAM capacitors, which have an inherently higher Q than MIM capacitors, were designed and implemented in this study. The effect of the capacitor Q versus frequency is presented in Fig. 2 for the Ka-band design mentioned above. Again, it is seen that, for $Q \sim 150$, there is a broad maximum around the design frequency.

TABLE I
EFFECT OF CAPACITOR Q ON LOSS PERFORMANCE ($C_s = 267$ fF AT X-BAND, $C_s = 93$ fF AT Ka-BAND). THE LOADED-LINE LOSS IS 28.7 dB/m AT X-BAND AND 99.7 dB/m AT Ka-BAND

Loss Component	X-band design	Ka-band design
Plated line loss	0.76 dB	0.51 dB
Evaporated line loss	0.24 dB	0.58 dB
19 Section Q loss	0.20 dB	0.39 dB
2 Section Q loss	0.43 dB	0.45 dB
Total max. loss	1.63 dB	1.93 dB
Measured max. loss	1.60 dB	2.10 dB

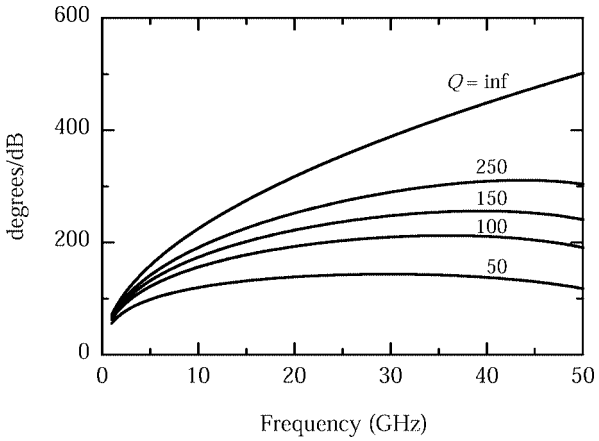


Fig. 2. Effect of the capacitor Q versus frequency for the Ka-band design.

There is another advantage to using MAM capacitors, i.e., physical size. Whereas a single MIM capacitor for X-band may be $25 \times 25\ \mu\text{m}^2$, the MAM capacitor is around $100 \times 100\ \mu\text{m}^2$. The capacitance requirements become much smaller at Ku- and Ka-band frequencies, making the MIM capacitors almost too small to fabricate, but MAM capacitors are quite easy to fabricate up to W-band and above.

III. Ka- AND X-BAND DMTL PHASE-SHIFTER DESIGN

Fig. 3 shows two unit cells of the Ka-band phase shifter on a quartz substrate ($\epsilon_r = 3.6$). The MAM capacitor is plated on three sides, thus providing a very high-Q, rigid, and stable capacitor (Fig. 4). The sacrificial layer underneath the MAM capacitor is polymethylmethacrylate (PMMA) and is defined using an oxygen plasma in a reactive ion etcher.

The impedance of the CPW unloaded line without the MAM cuts in the ground plane is approximately 98 Ω. However, fringing capacitance (2×9 fF) due to the ground-plane cuts lowers the t-line impedance to around 72 Ω. Test structures show that the combined Q of the fringing and MAM capacitance to be $\geq$250. Each MAM capacitor is approximately 24 fF and the fringing capacitance due to the ground-plane cuts is

[1]*Sonnet **em** Suite*, Sonnet ver. 6.0a, Sonnet Software Inc., Liverpool, NY, 1986–1998.

[2]*Advanced Design System* (ADS), ver. 1.3, Agilent Technol., San Jose, CA, 1983–1999.

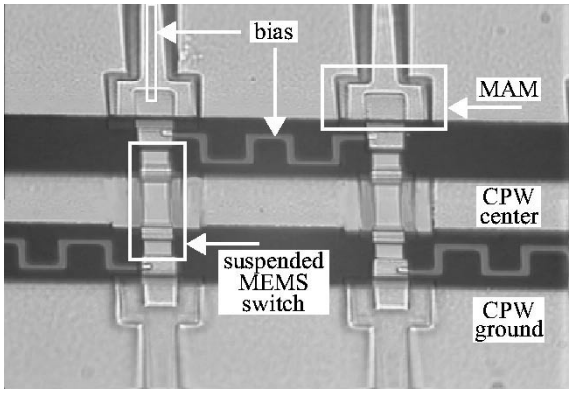


Fig. 3. Photograph of the Ka-band DMTL phase shifter showing two unit cells.

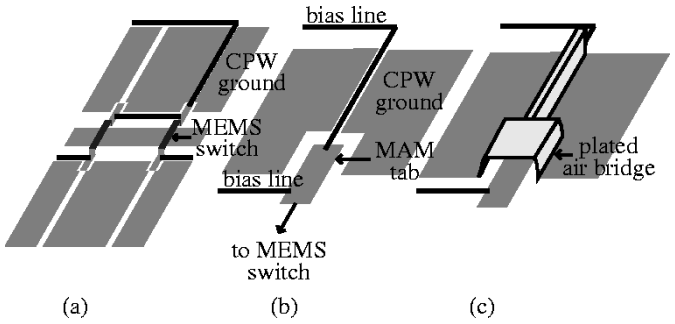


Fig. 4. Fabrication drawing of the MAM capacitor. (a) The bias line is run in a gap of the CPW ground at one point per bit and from there, runs in the CPW gap from switch to switch. (b) Detail drawing. (c) The complete MAM capacitor after a sacrificial layer over the MAM tab is removed, over which an air bridge was formed by electroplated gold.

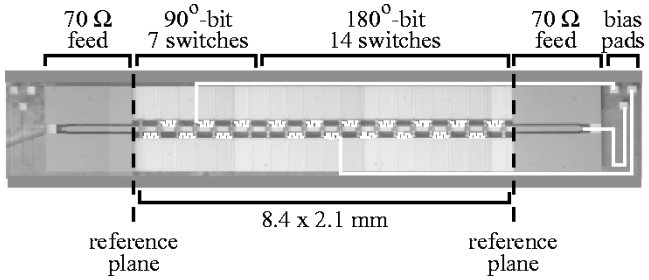
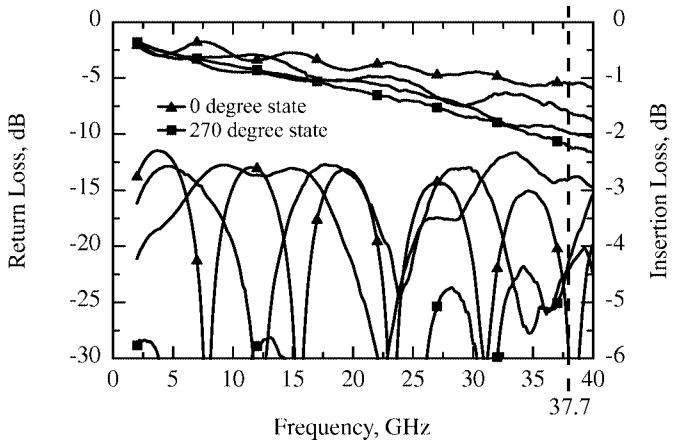


Fig. 5. Photograph of the Ka-band 2-bit 21-section DMTL phase shifter.

9 fF, resulting in a total loading capacitance of 66 fF. When the MEMS switches are activated, this loading lowers the CPW line impedance from 98 to 48 Ω.

A photograph of the entire Ka-band 2-bit phase shifter is shown in Fig. 5. It consists of two sections and each is connected to its own bias line. The first section has seven switches and is designed to have $\Delta\phi = 90°$ at 30 GHz. The second section has 14 switches and is designed to have $\Delta\phi = 180°$ at 30 GHz. Differential phase shifts of 90°, 180°, and 270° result from applying a ±20-V ac-bias voltage to the individual sections. The ac-bias voltage is needed to eliminate dielectric charging and to increase the lifetime of the MEMS switch to billions of cycles.

The X-band phase shifter is very similar to the Ka-band design, except that the design frequency is 10 GHz. The CPW line dimensions are 300/300/300 μm and the separation between MEMS switches is nearly three times larger ($s = 1150$ μm).



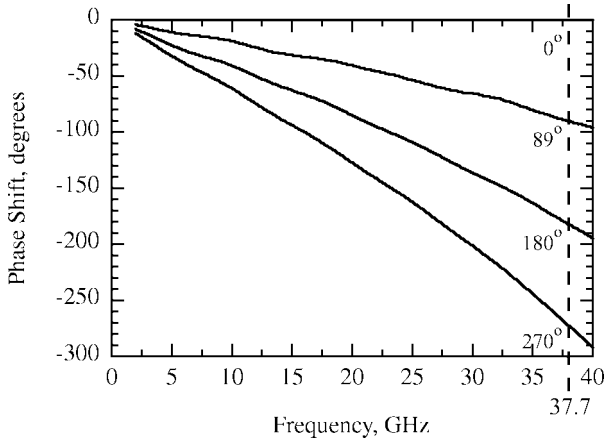


Fig. 6. Measurement of the Ka-band 2-bit DMTL phase shifter. Return loss is better than −11.5 dB and the average insertion loss is −1.5 dB at 37.7 GHz.

The impedance of the unloaded line without the MAM cuts in the ground plane is approximately 98 Ω. Each MAM capacitor is approximately 81.5 fF and the fringing capacitance due to the ground-plane cuts is 25 fF, resulting in a total loading capacitance of 213 fF. Again, when the MEMS switches are activated, this loading lowers the CPW line impedance from 98 to 46 Ω.

IV. Ka- and X-band 2-bit Measurements and Simulations

The Ka-band design was developed for a MEMS switch and a MAM capacitor with a height of 1.5 μm. The fabrication procedure used for the MEMS switch was changed in hopes of producing a lower stress switch and this was accomplished by removing certain metals from the switch. The resulting spring constant is 30 N/m with pull-in voltage of $V_p = 13$–14 V. The switching time is calculated to be 9 μs for a switching voltage of $V_s = 20$ V [11]. However, as a result of changing the fabrication procedure, the switch lowered to 1.2 μm after release, while the MAM capacitor remained at 2.1 μm, the PMMA sacrificial height. The movement is consistent over all 21 switches and was measured by a light-interferometer microscope. This measurement also shows that bowing and curling of the metal membrane to be less than 2000 Å, over its span and width. The MEMS switch up-state capacitance with a height of 1.2 μm is 232 fF

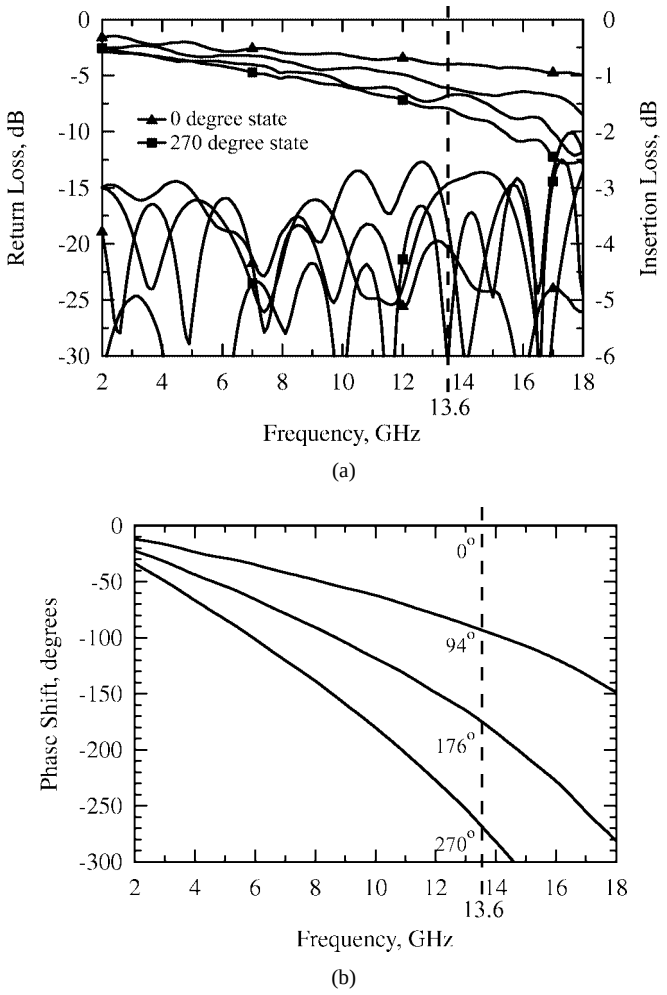


Fig. 7. Measurement of the X-band 2-bit DMTL phase shifter. Return loss is better than -12.5 dB, average insertion loss is -1.2 dB at 13.6 GHz where 94°, 176°, and 270° of phase shift is achieved.

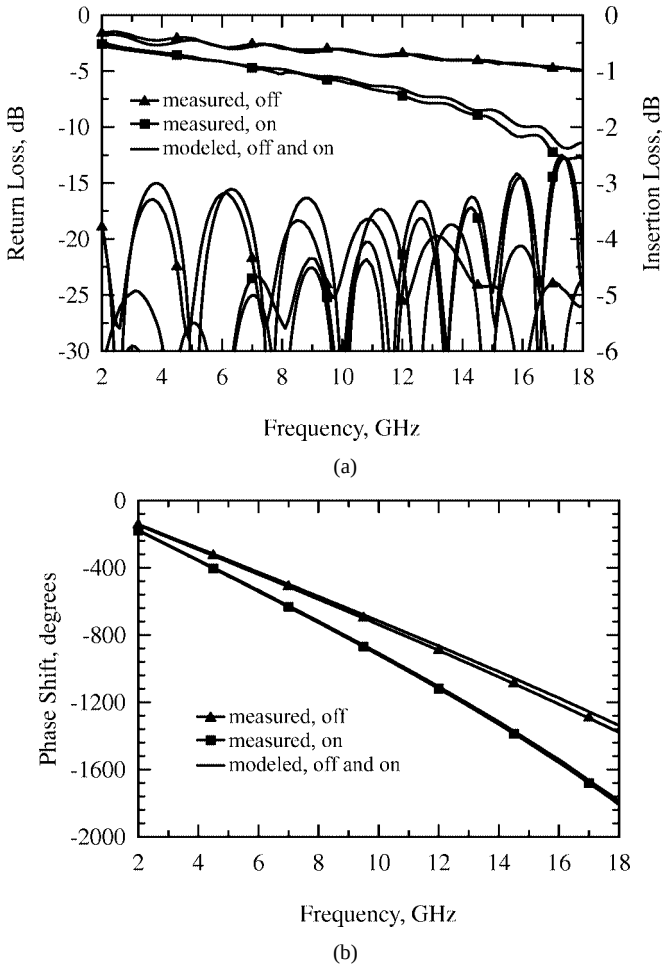


Fig. 8. X-band design measurement (with symbols) and simulation of the 21-switch DMTL phase shifter with all switches either on or off.

(X-band) and 58 fF (Ka-band). As a result, the loaded impedances are shifted from the ideal 60–42 to 58–46 Ω (X-band) and 62–48 Ω (Ka-band).

The measured phase shifter, therefore, does not operate at 30 GHz, but the distributed design is so wide band, that proper operation was achieved around 38 GHz. Fig. 6 shows the measured 2-bit performance with differential phase shifts of 89°, 180°, and 270° at 37.7 GHz. All states have a return loss of better than -11.5 dB, with a worst-case insertion loss of -2.1 dB. The average insertion loss is -1.5 dB. Simulation using a combined Sonnet/ADS method and using the new suspended heights agree quite well with measurements, as seen in [8].

The X-band phase shifter was also developed for a MAM and switch suspended height of 1.5 μm. The suspended height of the MEMS switch moved consistently, as it did in the Ka-band design, thus shifting the center frequency of the design from 10 to 13.6 GHz (Fig. 7). The measured differential phase shifts are 94°, 176°, and 270° at 13.6 GHz. All states have a return loss of better than -12.5 dB, a worst case insertion loss of -1.6 dB, and an average insertion loss of -1.2 dB. The simulations using the new suspended heights agree quite well with measurements (Fig. 8). Also modeled by the full electromagnetic (EM) simulation is the loss due to the thin-film Si–Cr bias resistor, whose effect is discussed in Section V.

V. Effect of the Bias Lines

Sonnet/ADS X-band simulations demonstrate that the 2-bit phase shifter would have a *maximum* insertion loss of -1.0 dB at 13.6 GHz if no bias lines were present, or if the resistances linking the bridges are increased significantly from 45 KΩ. Also, Ka-band simulations demonstrate the *maximum* insertion loss would be -1.1 dB at 37.7 GHz if the bias lines were removed. These losses should be compared to the measured *maximum* insertion losses of -1.6 and -2.1 dB at 13.6 and 37.7 GHz, respectively. This large influence on loss is caused by the bias lines and is explained below.

The biasing of each bit is achieved using a single high-resistance line, which is attached to one of the switches in the bit and then moving the bias from switch to switch using a meandering (Ka-band) or straight (X-band) thin-film high-resistance line (Figs. 3 and 4). Although the layout is near optimal, the bias lines still have a significant effect on the overall insertion loss performance of the phase shifter because they decrease the effective Q of the MAM capacitors.

The bias lines are sputtered from a silicon-chrome target, defined using wet etching (BHF) and are 20-μm wide,

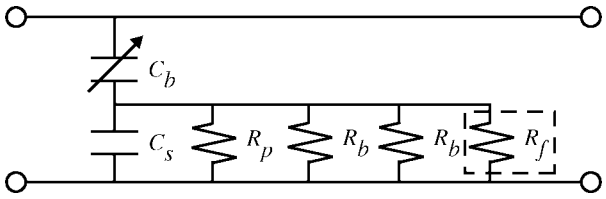


Fig. 9. Lumped model of DMTL section showing points where MAM Q is effectively reduced by bias lines. R_p is the loss due to the MAM Q. R_b is the effective resistance of the long bias line connecting the switches and R_f is the effective resistance of the bias line feed, which is present at only two out of 21 sections of the 2-bit phase shifter.

1500-Å thick, and approximately 610-μm long (Ka-band) and 1150-μm long (X-band). The conductivity of the material is 2150 S/m, thus resulting in a resistance of 23.7 KΩ (Ka-band) and 44.6 KΩ (X-band) from switch to switch. Effectively, the MAM capacitors "see" two of these resistances in parallel because there are two bias lines attached to each switch (Fig. 9). Additionally, where the bias lines feed underneath the CPW ground and contact the first switch in a phase bit, the capacitor Q is further reduced by another resistance in parallel with the two mentioned above. This small resistor is modeled as a 30-μm-long section of resistive line because the Si–Cr line strongly couples to the ground plane by means of the air bridge over it. The effective resistance of this short section is 1.16 KΩ.

The X-band design has a static MAM capacitance C_s of 213 fF and, using a Q of 400 at 13.6 GHz, $R_p = 33$ KΩ. By adding the resistance (R_b) of two parallel bias lines in parallel with R_p, the Q is effectively reduced from 400 to 160. The reduction in Q is most dramatic in the two sections of the phase shifter (out of 21) where the bias lines feed the MEMS switches. In this case, the Q is effectively reduced to around 15 (for a single section per phase bit). This reduction in the capacitor Q increases the maximum measured loss (when all switches are down) from an ideal value of -1.0 dB to the measured value of -1.6 dB at 13.6 GHz.

Similarly, the bias line influence on Ka-band performance can be explained. The static capacitance is $C_s = 66$ fF and using a Q of 300 at 37.7 GHz, $R_p = 19.2$ KΩ. By adding the resistance (R_b) of two parallel bias lines in parallel with R_p, the Q is effectively reduced from 300 to 110. The Q at the two points (out of 21) where bias lines are fed inside the CPW is reduced to around 15. Again, the reduction in the capacitor Q increases the maximum measured loss from an ideal value of -1.1 dB to the measured value of -2.1 dB at 37.7 GHz.

VI. Loss Components

There are three contributors to the insertion loss of the DMTL phase shifter:

1) line loss of the plated high-impedance line ($R_t = 255$ and $R_t = 875\ \Omega$/m at 13.6 and 37.7 GHz);
2) line loss of the thin high-impedance line underneath the MEMS switch ($R_t = 435$ and $R_t = 1{,}035\ \Omega$/m at 13.6 and 37.7 GHz);
3) Q loss of the MAM capacitors.

The influence of each of these contributors on the measured design is summarized in Table II. The plated and evaporated line losses are obtained from measured test structures. Each section of the X-band ($s = 1150$ μm) and Ka-band ($s = 400$ μm) DMTL includes a 200-μm-long evaporated section underneath each MEMS switch. The capacitor Q loss is all encompassing, including the reduction in MAM Q due to the bias lines. The loss in Table II is split into two parts: the first part details loss in the 19 sections, where there is a reduction in Q to 100–200 due to the bias lines. The second part details the loss in the remaining two sections, where the Q is greatly reduced by the bias line feeds under the CPW ground plane. It should be noted that, without bias lines, the loss of the DMTL phase shifter is essentially that of the plated and evaporated sections alone, as confirmed by simulations, because the Q of the MAM capacitors is quite high.

TABLE II
Loss Contributions (All Switches Down)

Q	R_p KΩ	Q loss (X) dB/m	Q loss (Ka) dB/m
inf	inf	0	0
250	14.9	11.8	35.8
150	8.9	19.7	59.7
100	6.0	29.5	89.7
50	3.0	59.0	99.7

VII. Conclusions

This paper presented very low-loss Ka- and X-band distributed phase shifters. The switch height was incorrect and this moved the design frequencies from 30 to 37.7 GHz and from 10 to 13.6 GHz. Still, the concept of using a very high-Q MAM capacitor in series with a low-loss MEMS switch is proven to work very well. The results present state-of-the-art performance for true-time-delay phase shifters at Ka-band frequencies. The design can be easily scaled to 45, 60, or 77 GHz for satellite and covert communications and radar systems.

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